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MICRO-FOUR-POINT PROBES IN A UHV SCANNING ELECTRON MICROSCOPE FOR *IN-SITU* SURFACE-CONDUCTIVITY MEASUREMENTS

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For *in-situ* measurements of surface conductivity in ultrahigh vacuum (UHV), we have installed micro-four-point probes (probe spacings down to 4 μm) in a UHV scanning electron microscope (SEM) combined with scanning reflection–high-energy electron diffraction (RHEED). With the aid of piezoactuators for precise positioning of the probes, local conductivity of selected surface domains of well-defined superstructures could be measured during SEM and RHEED observations. It was found that the surface sensitivity of the conductivity measurements was enhanced by reducing the probe spacing, enabling the unambiguous detection of surface-state conductivity and the influence of surface defects on the electrical conduction.

When two electrical leads [for example, outer probes in linear four-point-probe measurements as illustrated in Fig. 1(a)] are connected to a surface of a semiconductor crystal with a macroscopic spacing, and when a voltage is applied between them, the current I flows through three channels on/in the crystal: (1) surface-state bands on the topmost atomic layers (when surface superstructures are formed on the surface), (2) bulk-state bands in a surface space-charge layer beneath the surface (when bands bend), and (3) huge bulk-state bands in the inner crystal (independent of the surface conditions or treatments). A voltage drop V is measured by a pair of inner probes in Fig. 1(a) to obtain the four-point-probe resistance $R = V/I$, which contains the contributions from all of the above three channels. This four-point-probe method avoids contact resistances at the probe–sample contacts to get the sample resistance only, irrespective of whether the contacts are ohmic or Schottky-type. But it is impossible to separate the contributions of the three channels. Under the usual conditions in air, without surface superstructures on the surface, the measured resistance is interpreted as a bulk resistance. However, when bulk bands bend steeply beneath the surface to make an electron or hole accumulation layer (surface space-charge layer), or when conductive surface-state bands are created due to

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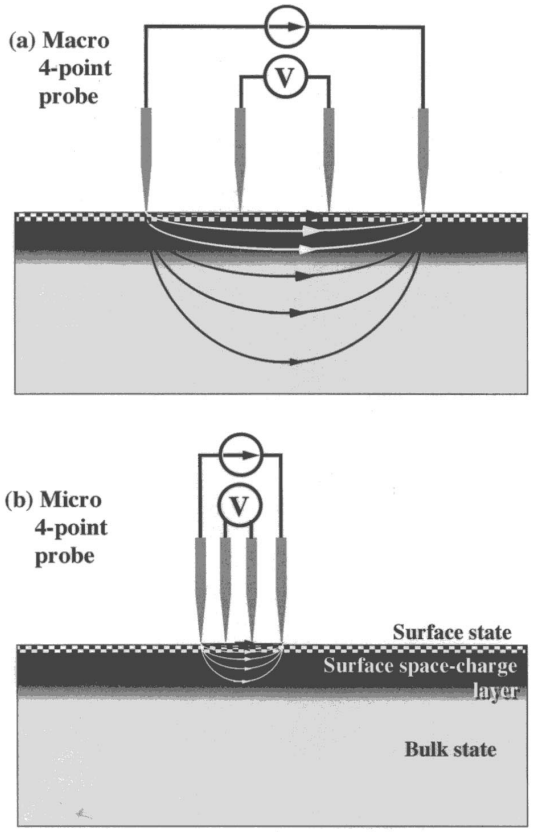

Fig. 1. Linear four-point-probe method in (a) macroscopic and (b) microscopic spacings, with schematic illustrations of current flow near a semiconductor surface.

well-ordered surface superstructures, the conductivity of the space-charge layers or surface-state bands cannot be ignored in the measured resistance. However, even in such cases, the surface-layer contributions are quite small because a large fraction of the current tends to flow through the interior bulk as shown in Fig. 1(a) when the probe spacing is a macroscopic distance.

By reducing the probe spacing as shown in Fig. 1(b), however, one can expect that a larger fraction of the current will flow near the surface, resulting in a more surface-sensitive measurement than by the macroscopic four-point probes.[1] The actual current distribution in the crystal is not so simple as shown in Fig. 1, because of a possible Schottky barrier between the surface states and the underlying bulk states[2] or a possible *pn* junction between the surface space-charge layer and the interior bulk. But the above simple expectation will be more or less true, as demonstrated in our measurements.

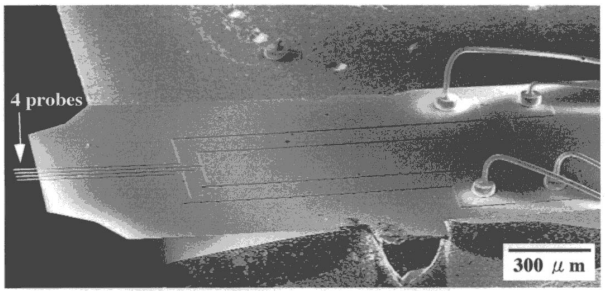

Fig. 2. A SEM image of a micro-four-point-probe chip.

This paper describes our micro-four-point-probe measurements combined with SEM–RHEED in UHV.

Figure 2 shows a SEM image of a micro-four-point-probe chip, developed at MIC of the Technical University of Denmark.[3,4] Such probes with 4, 8, 10, 20 and 60 μm spacings were made using silicon-based microfabrication technology following a procedure similar to that used to fabricate microcantilevers for atomic-force microscopy. The probes consist of four sharpened silicon oxide cantilevers extending from a silicon support chip. The silicon oxide paths on the chip are undercut, so that deposition of metal onto the chip results in conducting paths that are insulated from the support chip. The probes are very flexible, which makes the contact with sample surfaces straightforward even when the surface plane is not aligned with the probes.

The micro-four-point probes were integrated in a UHV SEM as illustrated in Fig. 3. This is a customized Hitachi S-4200 field-emission SEM enabling scanning RHEED and scanning reflection–electron microscopy (SREM) observations. The base pressure of this system was 2×10^{-8} Pa, while during metal deposition the pressure was kept below 1×10^{-7} Pa. Cleaning of the Si crystal surface by direct-current heating and metal depositions can be carried out on the SEM stage. In order to enhance the surface sensitivity, the primary electron beam irradiated the sample surface with a grazing incidence (about 10° from the surface), while RHEED observations were done with an angle of incidence less than 5°. Because of the grazing incidence of the primary electron beam, the SEM images shown here were foreshortened by a factor of about five in the vertical direction. The acceleration voltage of the electron beam was 30 kV

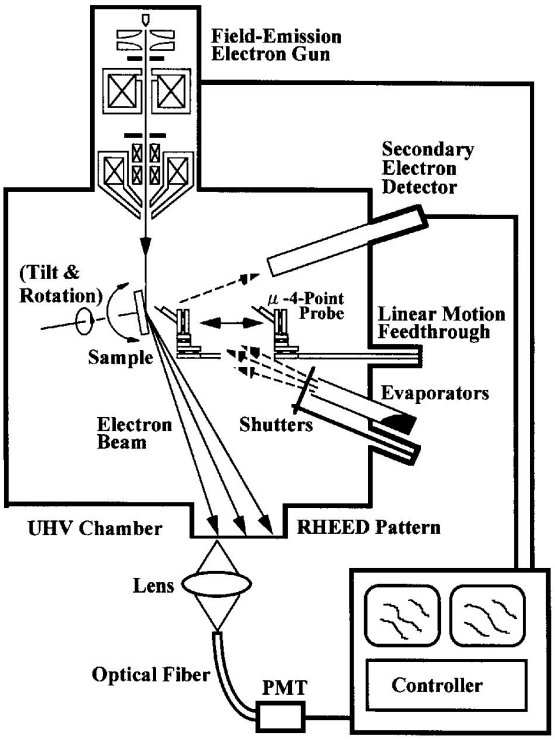

Fig. 3. An ultrahigh-vacuum scanning electron microscope with scanning RHEED and scanning reflection electron microscopy, equipped with metal evaporators. A micro-four-point-probe chip is mounted on three sets of piezoactuators in front of the sample surface, enabling precise positioning.

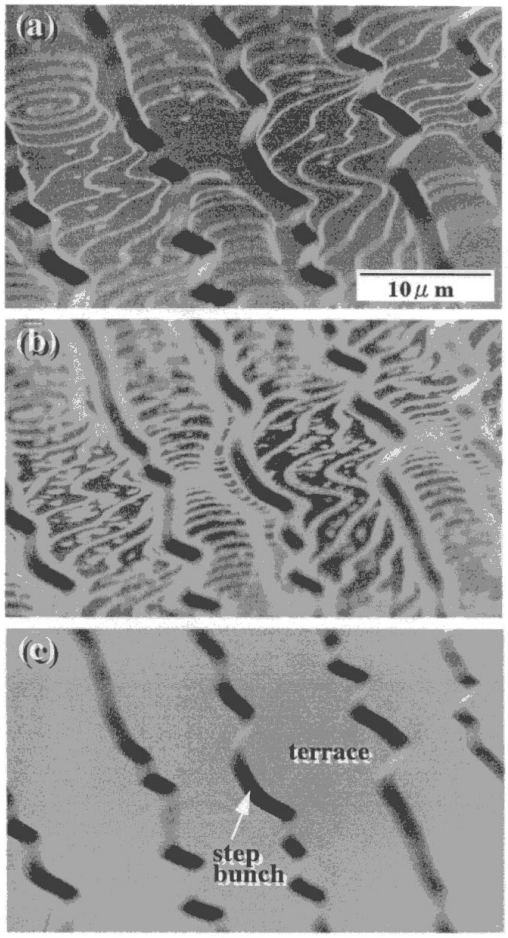

Fig. 4. Grazing-incidence scanning electron micrographs of a step-bunched Si(111) surface. (a), (b) Partially Ag-covered surface, coexisting with the 7×7 (dark areas) and $(\sqrt{3} \times \sqrt{3})$-Ag (bright areas) domains. Ag coverages are around 0.1 and 0.4 ML, respectively. (c) Wholly Ag-covered $(\sqrt{3} \times \sqrt{3})$-Ag surface with 1 ML Ag.

The beam diameter was about 2 nm on the sample surface.

The micro-four-point-probe chip was mounted on three sets of piezoactuators (Microslide, Omicron) for fine movements in XYZ directions, which enabled the probe positioning as precisely as about 10 nm accuracy with a 5 mm travel distance for each direction. The probes were made to approach the sample surface with an angle of about 20° from the surface with the aid of *in-situ* SEM observation, so that we could make gentle contact with the selected area on the surface. The probes were connected to a custom DC measurement system consisting of a current source and a high-precision amplifier outside the chamber. We guess that the probes destroy the surface superstructure at the contact points, so that the probes do not make direct contact with the surface-state bands of the superstructure — rather, only via bulk states. This will not be a fatal drawback to measuring voltage drops at the inner probes; equipotential lines should run and connect through bulk states to surface states.

In order to obtain an almost step-free area as wide as possible on a Si(111) sample surface, we used repeated flash-heating by direct current up to 1200°C for around one hour in total. After such treatment, the surface was separated into two regions, as shown in Fig. 4 — step-bunch regions around 2 μm wide and large flat terraces about 10 μm wide. Thirty to fifty atomic steps are bunched in the step-bunch regions, while only two or three monatomic steps run across the terrace regions. The monatomic steps are visualized as white lines in Fig. 4(a); a small amount of Ag deposition at 450°C decorated step edges.

The white region is a Si(111)-($\sqrt{3} \times \sqrt{3}$)-Ag superstructure, while the remaining dark areas are Si(111)-(7 × 7) clean domains. By increasing the Ag coverage up to one monolayer, the whole surface is covered by the ($\sqrt{3} \times \sqrt{3}$)-Ag superstructure, as shown in Fig. 4(c); the surface structures were confirmed by *in-situ* RHEED observations.

Sometimes, we used a patterned wafer to force the generation of large terraces in a more controllable way, developed by Ogino *et al.*[5] The patterning was done using a silicon laser etching facility; grids of small holes (1.5 μm in diameter, with a depth of around 1 μm) with spacings of 5, 10, 15 or 20 μm were etched with the laser, of which the total area was 1×1 mm^2. After flashing such wafers, the step bunches were roughly aligned to the position of the original hole grids; the holes themselves disappeared during the heating processes due to sublimation of Si atoms. The surface shown in Fig. 5 was prepared in this manner.

After preparation of the large terraces having the 7×7 clean structure or the ($\sqrt{3} \times \sqrt{3}$)-Ag structure, the micro-four-point probes were brought into contact with the silicon surface, as seen in Fig. 5, where an 8-μm-spacing probe chip was used. During the probe approach, all probes were grounded to avoid charging due to electron-beam irradiation of SEM. The total probe width is larger than the width of the terrace, so the outer probes are positioned on neighboring terraces. But, in Fig. 5(a), there is no step bunch running between the inner probes, measuring a voltage drop on an almost step-free terrace, while in Fig. 5(b) the inner probes measure a voltage drop across a step bunch. In this way, we can select the surface area under measurement by shifting the probe position with the Microslide, so that we can detect the effect of a step on the surface conductivity. Actually, we found that the resistance measured across a step bunch [Fig. 5(b)] was much larger than that measured on a terrace [Fig. 5(a)] with both the 7×7 and ($\sqrt{3} \times \sqrt{3}$)-Ag surfaces. This directly means that atomic steps on a surface cause an additional resistance, because carriers in the surface-state bands are scattered by step edges, as seen in a form of so-called electron standing waves near step edges[6] in the case of the ($\sqrt{3} \times \sqrt{3}$)-Ag surface, or because carriers in the surface space-charge layer are diffusely scattered at step edges (due to surface roughness) in the case of the 7×7 surface. The details will be reported elsewhere.

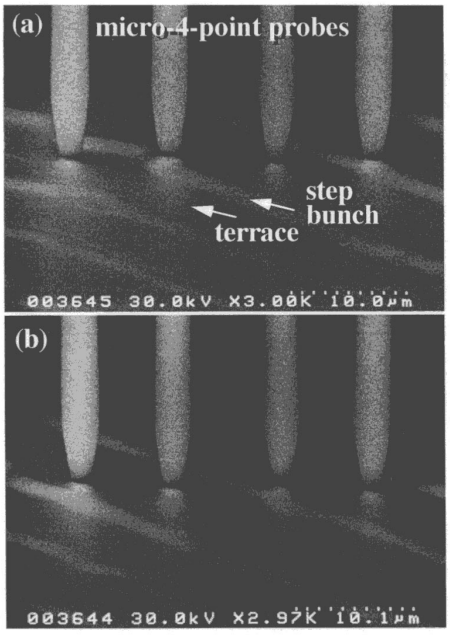

Fig. 5. Scanning electron micrographs showing the micro-four-point probes contacting a silicon surface. Slightly brighter bands on the surface are step bunches. The probes were shifted between (a) and (b).

We also compared the resistances between the two surface structures measured on a terrace like in Fig. 5(a). The resistance measured on the ($\sqrt{3} \times \sqrt{3}$)-Ag surface was smaller than that for the 7×7 clean surface by about two orders of magnitude. This should be compared with the result by macroscopic four-point probes of about 10-mm probe spacing, where the difference of resistance between the two surfaces was as small as about 10%.[7] These results mean that reducing the probe spacing makes the measurements more surface sensitive, as expected in Fig. 1.

By converting the measured resistances into sheet conductances, we confirmed that the extremely high conductance of the ($\sqrt{3} \times \sqrt{3}$)-Ag surface compared with that of the 7×7 surface is attributed to the surface-state band inherent in the superstructure, rather than the conductivity of the surface space-charge layer. Although this conclusion was already derived by macroscopic-four-point-probe measurements in UHV,[8] micro-four-point probes made it much more convincing. The details will be discussed elsewhere.

In summary, we have shown that the newly developed micro-four-point probes make it possible to measure the coductivity of selected surface areas with quite high surface sensitivity. We will be able to map the surface-conductivity distribution along a line or two-dimensionally by shifting the probes. This new tool will clarify the surface electronic transport properties much more directly than by macroscopic four-point probes.

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